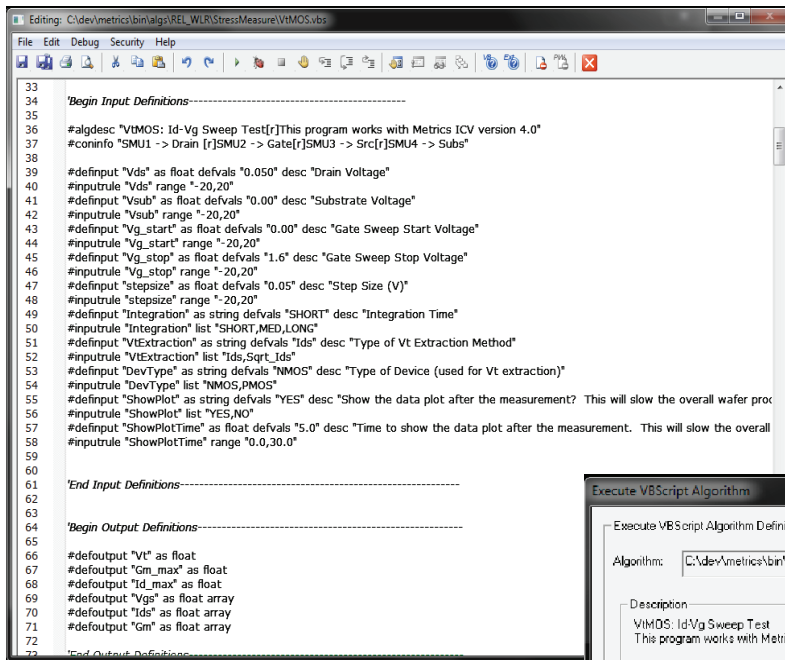


Point. Click. Measure. *It's as simple as that.*

Integrated Developer Environment

To simplify test development Metrics Technology offers an Integrated Developer Environment (IDE) which includes several libraries of functional APIs that provide access to the ICV Communication Server, Instrument Drivers, PGU/ Oscilloscope Drivers, as well as Thermal and Prober Driver templates. It includes algorithm suites for characterization of capacitors and devices for determining device process profiles and reliability of gate oxides and other stress induced failure mechanisms.

Using the Metrics IDE to create custom algorithms, device engineers can create sophisticated test methodologies, but provide just the right level of control for system users.

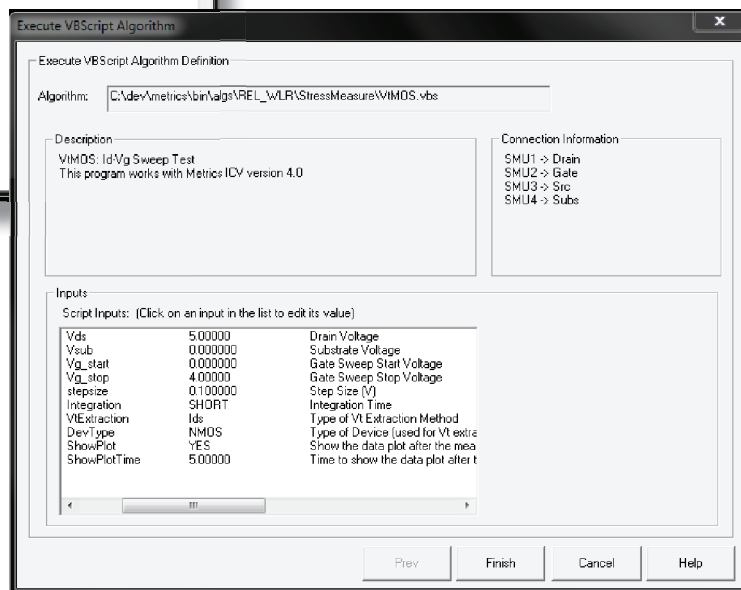


```

33
34
35 'Begin Input Definitions-----
36 #algdesc "VIMOS: Id-Vg Sweep Test[ ]This program works with Metrics ICV version 4.0"
37 #caninfo "SMU1 -> Drain [r]SMU2 -> Gate[r]SMU3 -> Src[r]SMU4 -> Subs"
38
39 #definput "Vds" as float defaults "0.050" desc "Drain Voltage"
40 #inputrule "Vds" range "-,20,20"
41 #definput "Vsub" as float defaults "0.00" desc "Substrate Voltage"
42 #inputrule "Vsub" range "-,20,20"
43 #definput "Vg_start" as float defaults "0.00" desc "Gate Sweep Start Voltage"
44 #inputrule "Vg_start" range "-,20,20"
45 #definput "Vg_stop" as float defaults "1.6" desc "Gate Sweep Stop Voltage"
46 #inputrule "Vg_stop" range "-,20,20"
47 #definput "stepsize" as float defaults "0.05" desc "Step Size [V]"
48 #inputrule "stepsize" range "-,20,20"
49 #definput "Integration" as string defaults "SHORT" desc "Integration Time"
50 #inputrule "Integration" list "SHORT,MED,LONG"
51 #definput "VtExtraction" as string defaults "Ids" desc "Type of Vt Extraction Method"
52 #inputrule "VtExtraction" list "Ids,Sqr_Ids"
53 #definput "DevType" as string defaults "NMOS" desc "Type of Device (used for Vt extraction)"
54 #inputrule "DevType" list "NMOS,PMOS"
55 #definput "ShowPlot" as string defaults "YES" desc "Show the data plot after the measurement? This will slow the overall wafer proc
56 #inputrule "ShowPlot" list "YES,NO"
57 #definput "ShowPlotTime" as float defaults "5.0" desc "Time to show the data plot after the measurement. This will slow the overall
58 #inputrule "ShowPlotTime" range "0.0,30.0"
59
60
61 'End Input Definitions-----
62
63
64 'Begin Output Definitions-----
65
66 #defoutput "Vt" as float
67 #defoutput "Gm_max" as float
68 #defoutput "Id_max" as float
69 #defoutput "Vgs" as float array
70 #defoutput "Ids" as float array
71 #defoutput "Gm" as float array
72
73 'End Output Definitions-----
  
```

VBScript Editor

The IDE license provides a full-featured script editor with syntax assistance, an interactive test execution environment and a comprehensive debugger. The developer can create VBScripts for entering user-defined inputs and outputs, sending low-level GPIB instrument-specific command strings, and implementing test branching. In addition the developer can use the included math libraries to perform parameter extraction and collection.



For more information:
www.metricstech.com
or
(505) 761-9630

Algorithms Suite

CV Algorithms

CVCalibration
CVFrequencySweep
CVBiasSweep
CVBiasSweep_with_Hysteresis
CVTimeSweep
CVSinglePoint
CVMinimumPhaseAngle
CV2FrequencyMeasurement

Description

Calibration functions for the supported meters.
A sweep of the oscillator bias while measuring.
A sweep of the DC bias while measuring device.
A sweep of the DC bias with hysteresis while measuring device.
A measurement of device parameters as a function of time.
A single point measurement of device parameters.
A sweep of the Impedance and Phase Angle to extract C.
A measurement of Impedance and Phase Angle at two frequencies to extract capacitance versus bias.

WLR - Oxide Algorithms

J_RAMP – Current Ramp

V_RAMP – Voltage Ramp

V_TDDDB – Constant Voltage Time to Breakdown

I_TDDDB – Constant Current Time to Breakdown

V_SILC – Constant Accelerated Voltage – Stress Induced Leakage Current

Description

A current ramp test that increases the applied current to the Gate while measuring the charge (Qacc) and voltage.
A voltage ramp test that increases the applied voltage to the Gate while measuring the charge (Qacc) and current.
A constant voltage is applied to the device while the resulting current is monitored for breakdown.
A constant current is applied to the device while the resulting voltage is monitored for breakdown.
A constant accelerated stress voltage is applied to the device while the resulting current is monitored for breakdown.

WLR - Stress/Measure Algorithms

HCI – Hot Carrier Injection
VtMOS – V Threshold Calculation

Ispot – 4 Terminal Constant Bias
DCStress – 4 Terminal Constant Bias Stress

Gummel – Forward Synchronous Sweep
RGummel – Reverse Synchronous Sweep
ACStress – 4 Terminal AC Bias Stress
CP_CA – Charge Pumping Constant Amplitude

CP_VA – Charge Pumping Variable Amplitude

CP_VF – Charge Pumping Variable Frequency

NBTI – Negative Bias Temperature Instability and NBTI-On-The-Fly

Description

A combined algorithm that performs all functions of a traditional HCI test. This test sweeps the Gate voltage while applying a constant Drain voltage and extracts Vth.
This algorithm applies a bias to the device while measuring the current values. A constant accelerated DC stress voltage is applied to the device and current is monitored.
The Base-Emitter voltage is swept while the Collector voltage is held constant. The Base-Collector voltage is swept while the Emitter voltage is held constant. A constant accelerated AC stress voltage is applied to the device.
A constant amplitude AC signal is placed upon the gate of the device while the substrate current is measured.
A variable amplitude AC signal is placed upon the gate of the device while the substrate current is measured.
A variable frequency AC signal is placed upon the gate of the device while the substrate current is measured.
A combined algorithm that performs all functions of a traditional NBTI test.

NVM Capacitor Algorithms

NVMCycleCap
NVMPulseCap
NVMRampCycleCap
NVMRampPulseCap

Description

This algorithm applies write/erase pulse cycles to a capacitor.
This algorithm applies pulses to a capacitor.
This algorithm applies ramped write/erase pulse cycles to a capacitor.
This algorithm applies ramp pulses to a capacitor.

NVM Device Algorithms

NVMCycleDev
NVMPulseDev
NVMRampCycleDev
NVMRampPulseDev

Description

This algorithm applies write/erase pulse cycles to an NVM device.
This algorithm applies pulses to an NVM device.
This algorithm applies ramped write/erase pulse cycles to an NVM device.
This algorithm applies ramp pulses to an NVM device.

Metrics Technology provided algorithms are based on JEDEC standards. Most of these algorithms have been verified using test structures provided by our partners or customers. Please refer to our website for the most current system requirements and instrument support.

Results from some algorithms may vary due to instrument performance or test structure designs. Full source code to the algorithms is provided to support user-defined enhancements. An annual license is required due to the additional support necessary to assist the end-user in making modifications.