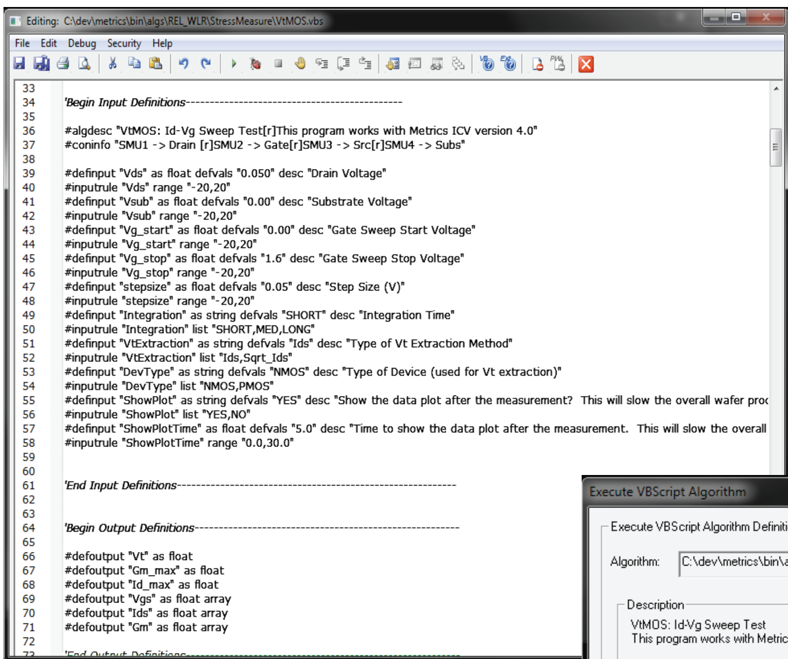
METRICS™
IDE Integrated Developer Environment

Point. Click. Measure. ***It's as simple as that.***

Integrated Developer Environment

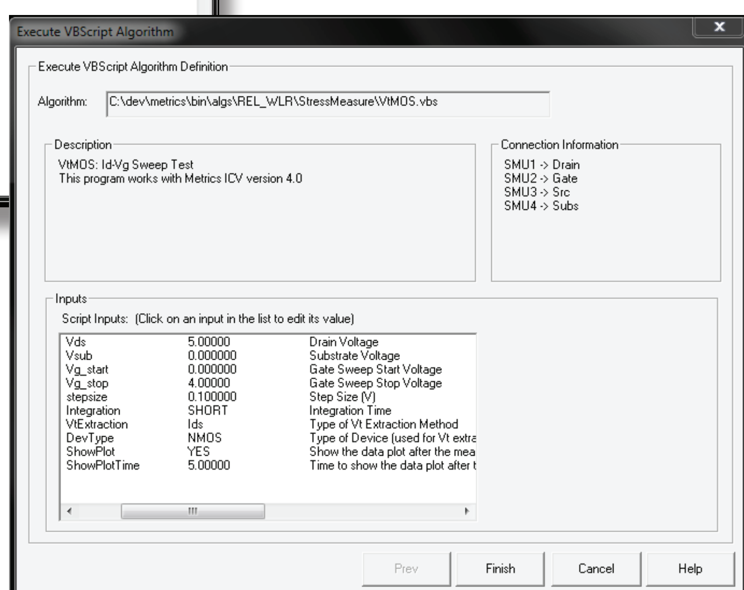
To simplify test development Metrics Technology offers an Integrated Developer Environment (IDE) which includes several libraries of functional APIs that provide access to the ICV Communication Server, Instrument Drivers, PGU/ Oscilloscope Drivers, as well as Thermal and Prober Driver templates. It includes algorithm suites for characterization of capacitors and devices for determining device process profiles and reliability of gate oxides and other stress induced failure mechanisms.

Using the Metrics IDE to create custom algorithms, device engineers can create sophisticated test methodologies, but provide just the right level of control for system users.



VBScript Editor

The IDE license provides a full-featured script editor with syntax assistance, an interactive test execution environment and a comprehensive debugger. The developer can create VBScripts for entering user-defined inputs and outputs, sending low-level GPIB instrument-specific command strings, and implementing test branching. In addition the developer can use the included math libraries to perform parameter extraction and collection.



For more information:

www.metricstech.com
or
(505) 761-9630

Algorithms Suite

CV Algorithms	Description
CVCalibration	Calibration functions for the supported meters.
CVFrequencySweep	A sweep of the oscillator bias while measuring.
CVBiasSweep	A sweep of the DC bias while measuring device.
CVBiasSweep_with_Hysteresis	A sweep of the DC bias with hysteresis while measuring device.
CVTimeSweep	A measurement of device parameters as a function of time.
CVSinglePoint	A single point measurement of device parameters.
CVMinimumPhaseAngle	A sweep of the Impedance and Phase Angle to extract C.
CV2FrequencyMeasurement	A measurement of Impedance and Phase Angle at two frequencies to extract capacitance versus bias.

WLR - Oxide Algorithms	Description
J_RAMP – Current Ramp	A current ramp test that increases the applied current to the Gate while measuring the charge (Qacc) and voltage.
V_RAMP – Voltage Ramp	A voltage ramp test that increases the applied voltage to the Gate while measuring the charge (Qacc) and current.
V_TDDB – Constant Voltage Time to Breakdown	A constant voltage is applied to the device while the resulting current is monitored for breakdown.
I_TDDB – Constant Current Time to Breakdown	A constant current is applied to the device while the resulting voltage is monitored for breakdown.
V_SILC – Constant Accelerated Voltage – Stress Induced Leakage Current	A constant accelerated stress voltage is applied to the device while the resulting current is monitored for breakdown.

WLR - Stress/Measure Algorithms	Description
HCI – Hot Carrier Injection	A combined algorithm that performs all functions of a traditional HCI test.
VtMOS – V Threshold Calculation	This test sweeps the Gate voltage while applying a constant Drain voltage and extracts Vth.
Ispot – 4 Terminal Constant Bias	This algorithm applies a bias to the device while measuring the current values.
DCStress – 4 Terminal Constant Bias Stress	A constant accelerated DC stress voltage is applied to the device and current is monitored.
Gummel – Forward Synchronous Sweep	The Base-Emitter voltage is swept while the Collector voltage is held constant.
RGummel – Reverse Synchronous Sweep	The Base-Collector voltage is swept while the Emitter voltage is held constant.
ACStress – 4 Terminal AC Bias Stress	A constant accelerated AC stress voltage is applied to the device.
CP_CA – Charge Pumping Constant Amplitude	A constant amplitude AC signal is placed upon the gate of the device while the substrate current is measured.
CP_VA – Charge Pumping Variable Amplitude	A variable amplitude AC signal is placed upon the gate of the device while the substrate current is measured.
CP_VF – Charge Pumping Variable Frequency	A variable frequency AC signal is placed upon the gate of the device while the substrate current is measured.
NBTI – Negative Bias Temperature Instability and NBTI-On-The-Fly	A combined algorithm that performs all functions of a traditional NBTI test.

NVM Capacitor Algorithms	Description
NVMCycleCap	This algorithm applies write/erase pulse cycles to a capacitor.
NVMPulseCap	This algorithm applies pulses to a capacitor.
NVMRampCycleCap	This algorithm applies ramped write/erase pulse cycles to a capacitor.
NVMRampPulseCap	This algorithm applies ramp pulses to a capacitor.

NVM Device Algorithms	Description
NVMCycleDev	This algorithm applies write/erase pulse cycles to an NVM device.
NVMPulseDev	This algorithm applies pulses to an NVM device.
NVMRampCycleDev	This algorithm applies ramped write/erase pulse cycles to an NVM device.
NVMRampPulseDev	This algorithm applies ramp pulses to an NVM device.

Metrics Technology provided algorithms are based on JEDEC standards. Most of these algorithms have been verified using test structures provided by our partners or customers. Please refer to our website for the most current system requirements and instrument support.

Results from some algorithms may vary due to instrument performance or test structure designs. Full source code to the algorithms is provided to support user-defined enhancements. An annual license is required due to the additional support necessary to assist the end-user in making modifications.